KBR ACADEMY · FREE PUBLIC SAMPLE · READ-ONLY DATA SHEETS

Lab data sheets: reverse-engineer an unbranded hub-motor controller

KBR Academy · Companion to `controllers-reverse-engineering-unbranded` · 180 minutes

These are blank, printable sheets for the lab. They are part of the **free public sample** and may be downloaded and filled in on paper or on a copy of this file.

- **Submitting** the lab and getting assessor sign-off stay with the paid course.
- **Doing** the practical work (energising a controller, connecting a pack, or any other powered work) requires you to pass the Foundations Safety Gate first. Reading or printing these sheets does not waive that requirement.
- Numeric pass thresholds below are **KBR lab criteria for the supplied kit**, not industry standards.

Name / student id: _____ Date: _____ Kit / CUT id: _____

Part 0 — Safety gate (complete before any measurement)

An unsafe act at any point is an automatic fail. Assessor countersign is part of the paid, assessed lab.

#	Check	Done (initials)	Assessor
0.1	Pack isolated, terminals capped, staged on a non-combustible surface away from the bench		
0.2	Bench supply fused; current limit set to 0.3 A; output OFF		
0.3	CUT bus capacitors discharged through the discharge tool		
0.4	B+ to B− measured with DMM: _____ V (must be under 1 V)		
0.5	Scope ground strategy written down (which probes are differential or isolated, and which are single-ended — and why that is safe)		
0.6	PPE on; jewellery removed; extinguisher, sand or blanket within reach; exit clear		
0.7	Second person present		

Scope ground strategy:

_____

Assessor countersign: _____ Date/time: _____

Part 1 — Teardown and visual identification

Photograph the case, labels, every connector face, and both PCB sides.

Data sheet 1: component identification

Look up each **manufacturer datasheet**. Record the URL.

Block	Reference / marking	Manufacturer & part (if identifiable)	Key ratings from datasheet	Datasheet URL
MCU			Core, supply V, debug interface	
Gate driver(s)			Max supply / offset voltage	
MOSFETs (count: ____)			V(BR)DSS, RDS(on) @10 V, VGS(th), VSD	
Bus capacitors (count / value / V)			µF, V, temp rating	
Current sensing (shunt or Hall-effect IC)			DC-link shunt, phase shunts, and/or a Hall-effect current-sensor IC (e.g. ACS711)? Evidence of a shunt mod?	
Regulator(s)			Input max V, output V	

Design ceiling. Lowest-rated part on the HV rail: _____ rated _____ V.

Maximum safe pack (series count, full-charge V): _____. Does the case label agree? Y / N

KBR shop rule (our practice, not a standard): FETs and capacitors rated at least 1.2× the full-charge pack voltage; prefer more if regen is used.

Part 2 — Connector pin identification

Record colours, but label them as "this unit only". Wire colour is a hint, never proof.

2a. Unpowered (capacitors discharged)

Test	Expected signature	Reading	Pin(s) identified
B+ to B− (ohms or diode)	Capacitor charging, reading climbs		B+ = ____ B− = ____
Phase → B+ (red on phase, black on B+), ×3	A diode-junction reading, equal on all three phases (record your meter's value)	U ____ V ____ W ____	
B− → phase (red on B−, black on phase), ×3	A diode-junction reading, equal on all three phases (record your meter's value)	U ____ V ____ W ____	
Reverse of each of the above	OL or slow capacitor charging		
Phase-to-phase ×3	Not a short		

Thin pins to B− (continuity)	Low resistance on logic-ground candidates (record the value; not every board ties them directly to B−)		
Candidate Hall signals to GND	Three identical readings		

2b. Powered (current limit 0.3 A, nominal voltage)

Idle current: _____ mA. Thermal check after 60 s: OK / hot spot at _____.

Pin / wire colour	Connector	Voltage to GND (idle)	Behaviour when exercised	Function identified

Rails (measure; do not assume): gate-drive ____ V; 5 V ____ V; 3.3 V ____ V (if present).

Deliverable: a hand-drawn connector diagram for each plug (face view, latch orientation marked), with pin functions.

Part 3 — Motor characterisation (motor DISCONNECTED from the CUT)

3a. Mechanical / electrical integrity

Test	Result	Pass?
Free spin, phases separated	Free / drag	
Two phases shorted: drag equal across all three pairs?	1–2 ___ 2–3 ___ 3–1 ___	
Phase-pair resistance by I–V (I = ____ A)	1–2 ____ mΩ 2–3 ____ mΩ 3–1 ____ mΩ; spread ____ %	
Insulation phase / Hall to axle		

3b. Hall table (Halls powered from 5 V with pull-ups; wheel turned slowly forward)

Step	Hall A (wire colour _____)	Hall B (_____)	Hall C (_____)
1			
2			
3			
4			
5			
6			

Hall supply current: ____ mA. Spacing: 120° / 60° (justify): _____

Gray code (exactly one bit changes per step)? Y / N. Any stuck sensor? _____

3c. Pole pairs and back-EMF

- Hall A cycles per wheel revolution: ____ → pole pairs ____
- BEMF line-to-line Vpk at ____ rpm: 1–2 ____ V, 2–3 ____ V, 3–1 ____ V. Imbalance ____ %
- Second speed ____ rpm: Vpk ____ V. Ke = ____ V/rpm (linearity check: ____ %)
- BEMF shape: trapezoidal / sinusoidal (attach scope capture)

3d. Motor table for Method B

For each Hall state, record the line-to-line pair that is most positive (+wire / −wire). Do not assume Hall edges line up with back-EMF zero crossings.

Hall state (ABC)	Line-to-line BEMF most positive (+wire / −wire)

Part 4 — Controller table and mapping

4a. Controller table

CUT into the star resistor load, Hall emulator on the Hall inputs, lowest supply voltage above LVC, current limit 0.5 A, small throttle.

Hall input state (controller labels)	Phase out 1	Phase out 2	Phase out 3	High / Low / Float

Stall-protection behaviour (if any): _____

4b. Solve (Method B)

Motor Hall wire → controller Hall input: A→____ B→____ C→____

Motor phase wire → controller phase output: 1→____ 2→____ 3→____

Working (which states you matched first and why):

_____
_____

4c. Confirm (gentle spin, current limit 2–3 A, wheel clear)

Mapping	Direction	Smooth?	No-load current @ fixed throttle
Method B solution			
One cyclic phase rotation of it			
One phase swap of it			

4d. Method A cross-check (6 × 6 grid)

Mark F (forward-smooth), R (reverse-smooth), X (rough / no spin), or the current reading. Rows are phase orders; columns are Hall orders. *The assessor may direct you to complete only one row and one column if time is short.*

Phase \\ Hall	H1	H2	H3	H4	H5	H6
P1						
P2						
P3						
P4						
P5						
P6						

Part 5 — Bench test (KBR criteria for the supplied kit)

Follow lesson Section 9.

Check	Measured	Pass criterion (KBR kit criteria)	Pass?
Idle current		No current-limit trip; within ±25% of the KBR baseline for this kit controller	
Gate-drive rail		Within ±10% of the value established in Part 2 and stable	
5 V rail		4.75–5.25 V with all peripherals connected	
Throttle idle / full at controller		Idle below the controller's start threshold; full within the range the controller accepts	
Brake input		Drive ceases within 0.5 s of brake activation, every time (5 trials)	
Gate PWM present in all six positions		Yes, in every leg (scope captures attached)	
Known-good motor spin @ 2–3 A limit		Smooth, forward, no current-limit trip	
Customer motor no-load current		Within ±15% of the known-good motor at the same throttle/speed **and** lowest of the tested mappings	
Thermal after 5 min no-load run		No component above 60 °C (thermal camera or probe)	

Part 6 — Report and recommendation (up to one page)

Attach the pin-function diagram. Then write:

1. Design ceiling and whether the unit is correctly rated for the target pack.
2. Motor summary: pole pairs, Hall spacing, BEMF shape, Ke, integrity.

3. Final mapping and evidence.
4. Repair vs replace decision against the lesson Section 11 criteria. If replacing, give a full replacement specification (voltage, battery current vs BMS, phase current, sensored / dual-mode, Hall spacing, drive type, display protocol, brake polarity, PAS type, connectors, legal configuration under B.C. Reg. 64/2024).

Overall pass criteria (assessed lab, paid)

- Part 0 completed and countersigned **before** any measurement. An unsafe act at any point is an automatic fail.
- At least 90% of connector pins correctly identified, with **all** power, phase, Hall and brake pins correct.
- Correct Hall spacing and pole-pair count.
- Method B mapping correct, confirmed by the lowest no-load current.
- All Part 5 checks pass.
- The recommendation is technically justified and includes any legal configuration notes.

Extension (optional, merit grade)

Capture the display UART with a logic analyser. Report the baud rate, frame length, repetition interval and which byte(s) change with the assist level and the brake. Do not transmit to the controller. Scope the idle level before connecting an adapter; do not assume 5 V TTL.